



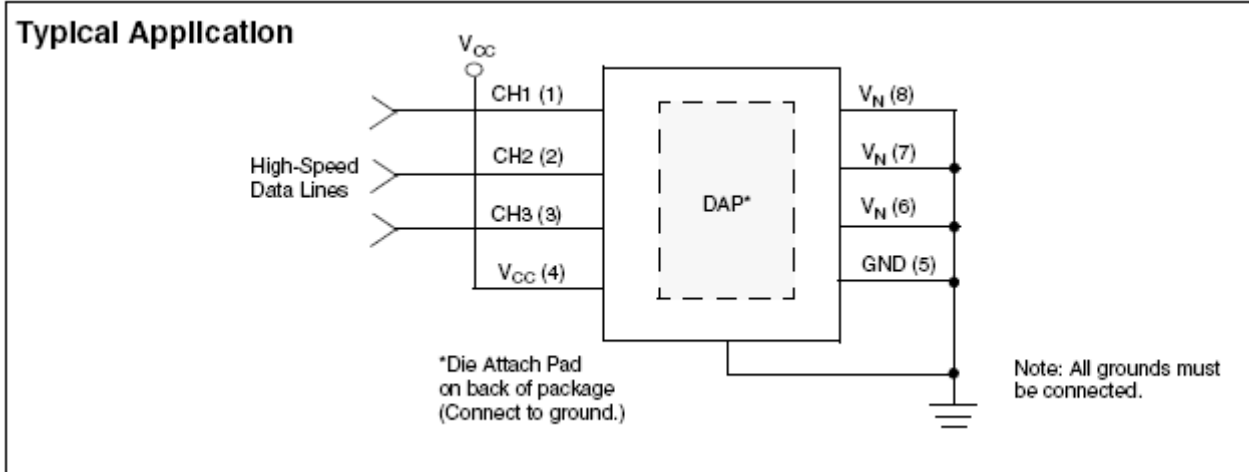
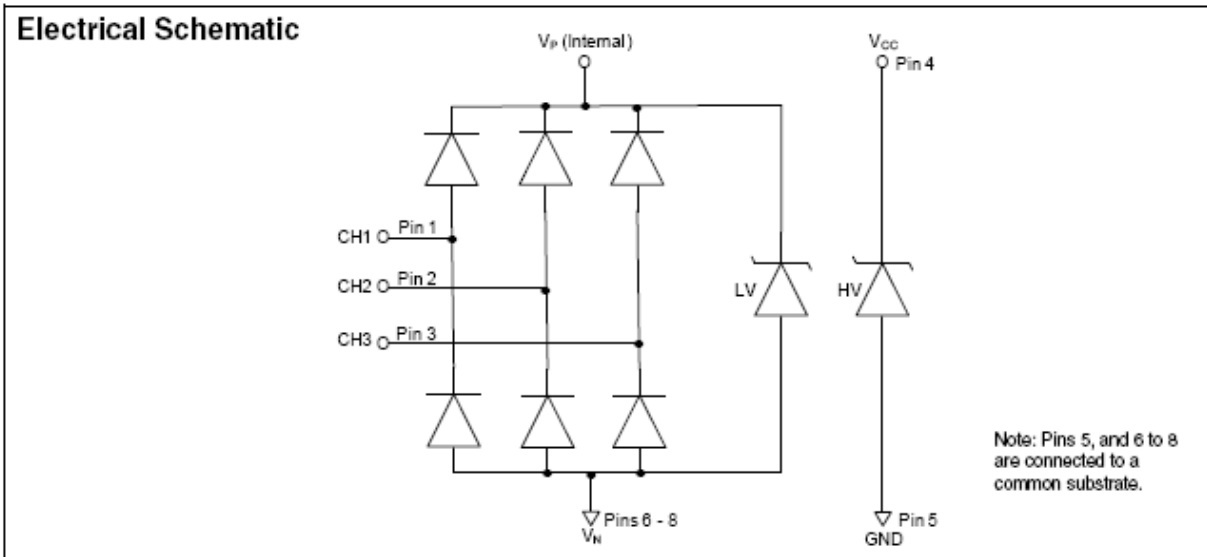
4-Channel Low Capacitance Dual-Voltage ESD Protection Array

CM1641

Features

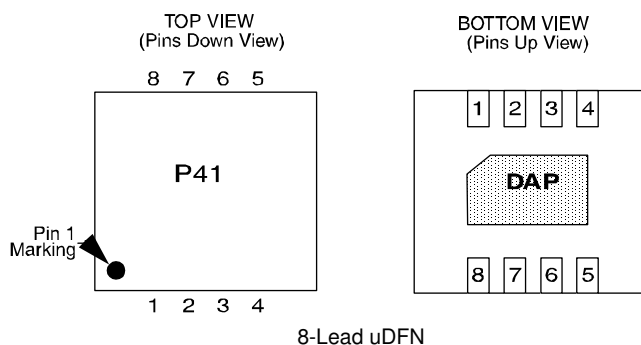
- Three channels of low voltage ESD protection
- One channel of high voltage ESD protection
- Provides ESD protection to IEC61000-4-2 Level 4:
±8kV contact discharge (Pins 1-3)
±15kV contact discharge (Pin 4)

- Low channel input capacitance
- Minimal capacitance change with temperature and voltage
- High voltage zener diode protects supply rail
- No need for external bypass capacitors
- Each I/O pin can withstand over 1000 ESD strikes*
- RoHS compliant, lead-free finish



*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ±8kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

PACKAGE / PINOUT DIAGRAMS



Note: These drawings are not to scale.

Pin Descriptions

4-CHANNEL, 8-LEAD, UDFN-8 PACKAGE

Pin	Name	Type	Description
1	CH1	I/O	LV Low-capacitance ESD Channel
2	CH2	I/O	LV Low-capacitance ESD Channel
3	CH3	I/O	LV Low-capacitance ESD Channel
4	V_{CC}	HV V_{DD}	HV ESD Channel
5	GND		Ground
6	V_N		Negative Voltage Supply Rail
7	V_N		Negative Voltage Supply Rail
8	V_N		Negative Voltage Supply Rail
DAP	GND		Die Attach Pad (Ground)

CM1641

Ordering Information

PART NUMBERING INFORMATION				
# of Channels	Leads	Package	Lead-free Finish	
			Ordering Part Number ¹	Part Marking
4	8	UDFN-8, 0.4mm	CM1641-04D4	P41

Note 1: Parts are shipped in Tape and Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
DC Voltage on Low-voltage Pins	6.0	V
DC Voltage on High-voltage Pins (V_{CC} pin)	14.5	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C

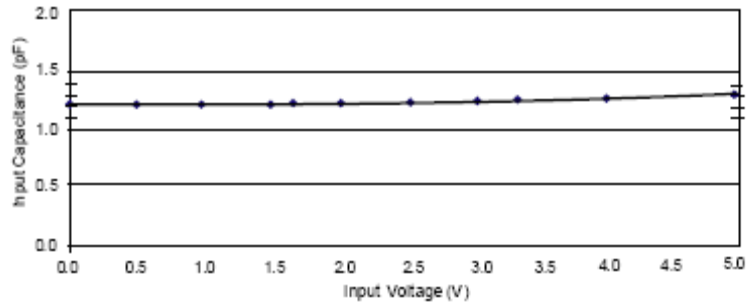
ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _F	LV Diode Reverse Voltage (Positive Voltage)	I _F = 10mA; T _A = 25 °C	6.8	8.2	9.2	V
	LV Diode Forward Voltage (Negative Voltage)	I _F = 10mA; T _A = 25 °C	-1.05	-0.9	-0.6	V
I _{LEAK}	LV Channel Leakage Current	T _A = -30 °C to 65 °C; V _{IN} = 3.3V, V _N = 0V			100	nA
C _{IN}	LV Channel Input Capacitance	At 1 MHz, V _N = 0V, V _{IN} = 1.65V		1.2	1.5	pF
ΔC _{IN}	LV Channel Input Capacitance Matching	At 1 MHz, V _N = 0V, V _{IN} = 1.65V		0.02		pF
I _{LEAK_HV}	HV Channel Leakage Current	T _A = 25 °C; V _{CC} = 11V, V _N = 0V		0.1	1.0	μA
C _{IN_HV}	HV Channel Input Capacitance	At 1 MHz, V _N = 0V, V _{IN} = 2.5V		53		pF
V _{F_HV}	HV Diode Breakdown Voltage Positive Voltage	I _F = 10mA; T _A = 25 °C	14.6		17.7	V
V _{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard	T _A = 25 °C	±8 (Pin 1-3) ±15 (Pin 4)			kV kV
V _{CL}	LV Channel Clamp Voltage (Pin 1-3) Positive Transients Negative Transients	T _A = 25 °C, I _{pp} = 1A, t _p = 8/20 μS		+9.64 -1.75		V V
R _{DYN}	Dynamic Resistance LV Channel Positive Transients LV Channel Negative Transients HV Channel Positive Transients HV Channel Negative Transients	I _{pp} = 1A, t _p = 8/20 μS Any I/O pin to Ground;		0.72 0.59 1.20 0.36		Ω Ω Ω Ω

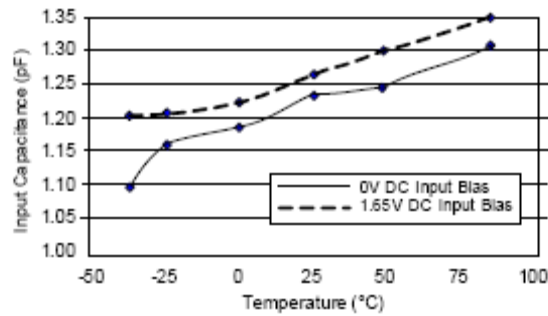
Note 1: All parameters specified at T_A = -40 °C to +85 °C unless otherwise noted.

Performance Information

Input channel capacitance performance curves for low voltage pins



Typical Variation of C_{IN} vs. V_{IN}
 (Low voltage inputs, $f=1\text{MHz}$, $V_N = 0\text{V}$)



Typical Variation of C_{IN} vs. Temp
 (Low voltage inputs, $f=1\text{MHz}$, $V_N = 0\text{V}$)

Performance Information (cont'd)

Typical filter performance for low voltage pins

Nominal conditions unless specified otherwise, 50 ohm environment.

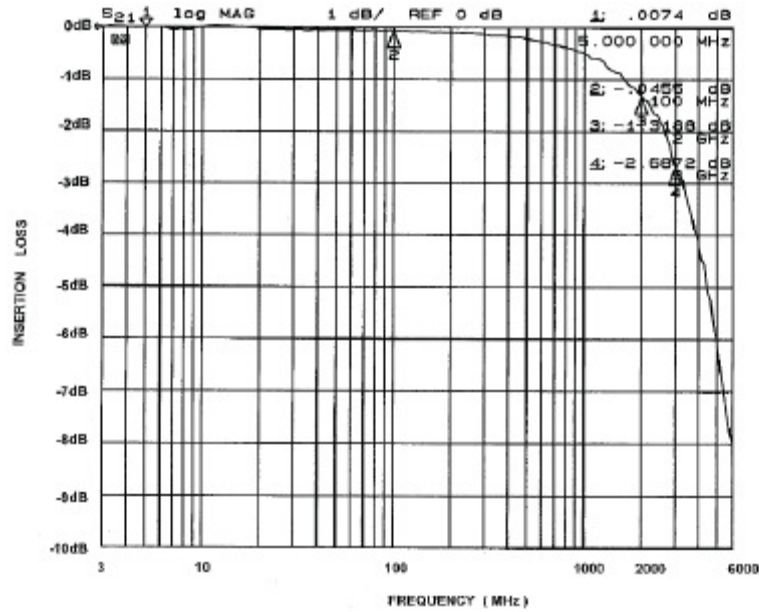


Figure 1. Channel 1 Vs. All GND Pins (0V DC Bias)

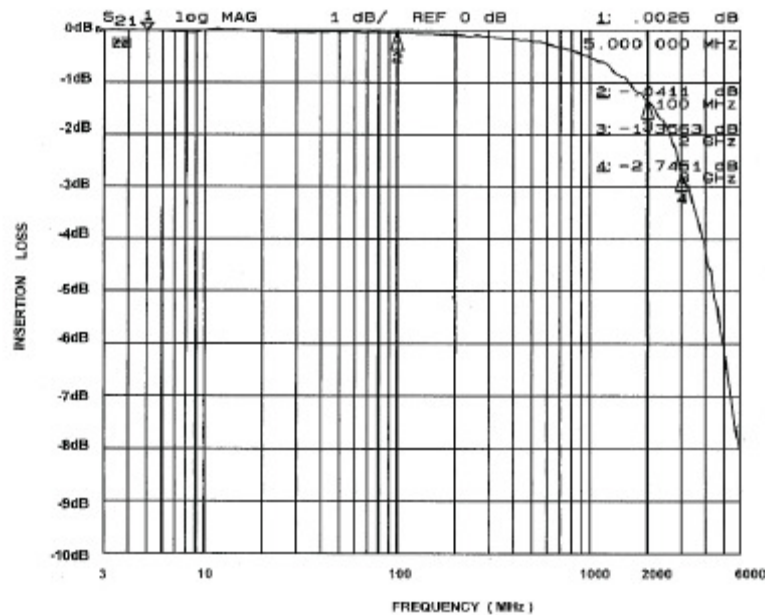


Figure 2. Channel 2 Vs. All GND Pins (0V DC Bias)

Performance Information (cont'd)

Typical filter performance for low voltage pins

Nominal conditions unless specified otherwise, 50 ohm environment.

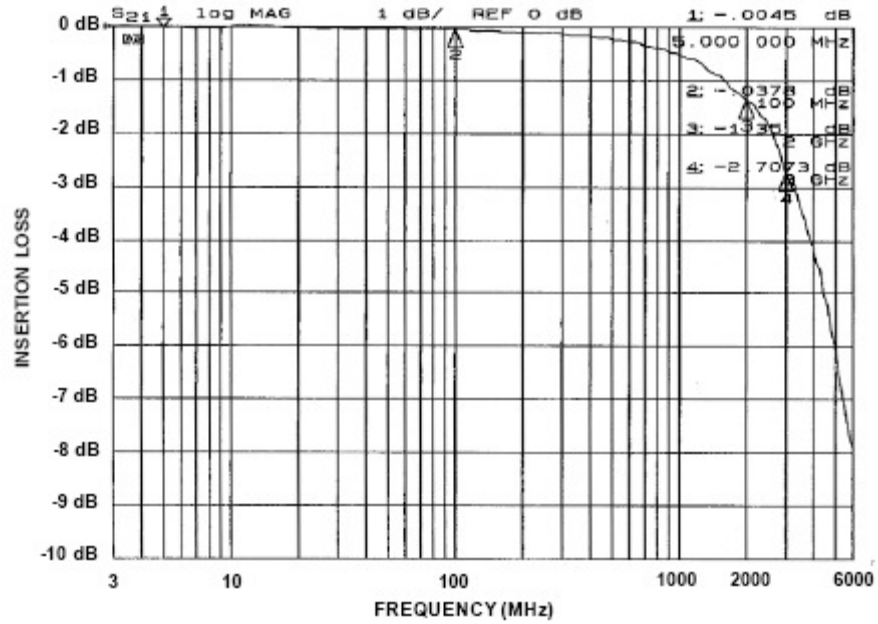


Figure 3. Channel 3 Vs. All GND Pins (0V DC Bias)

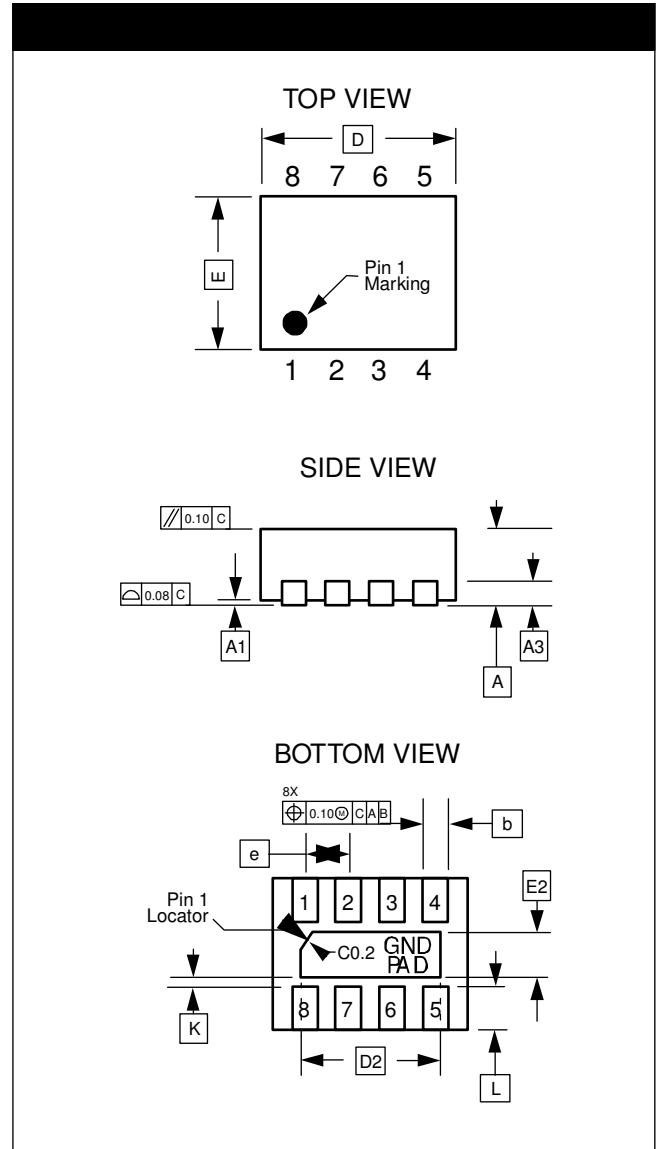
Mechanical Details

uDFN-08 Mechanical Specifications, 0.4mm

The 8-lead, 0.4mm pitch uDFN package dimensions are presented below.

PACKAGE DIMENSIONS						
Package	uDFN					
JEDEC No.	MO-229C*					
Leads	8					
Dim.	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.127 REF			0.005 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.60	1.70	1.80	0.063	0.067	0.071
D2	1.10	1.20	1.30	0.043	0.047	0.051
E	1.25	1.35	1.45	0.049	0.053	0.057
E2	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 BSC			0.016 BSC		
K	0.22 REF			0.009 REF		
L	0.15	0.25	0.35	0.006	0.010	0.014
# per tape and reel	3000 pieces					
Controlling dimension: millimeters						

* This package is compliant with JEDEC standard MO-229C with the exception of the D, D2, E, E2, K and L dimensions as called out in the table above.

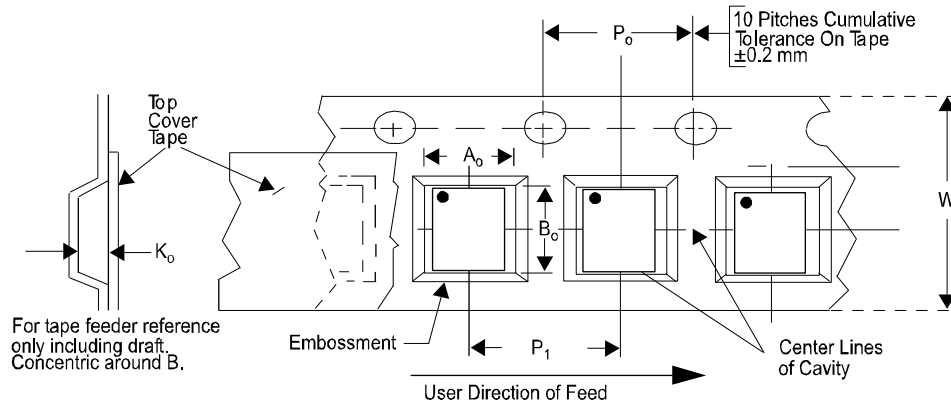



Dimensions for 8-Lead, 0.4mm pitch uDFN Package

CM1641

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) $B_o \times A_o \times K_o$	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_o	P_1
CM1641	1.70 X 1.35 X 0.50	1.95 X 1.60 X 0.60	8mm	178mm (7")	3000	4mm	4mm



ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855
Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative